DATA SHEET

TDA8046
Multi-mode QAM demodulator

Product specification
Supersededs data of 1996 Jul 23
File under Integrated Circuits, IC02

1996 Nov 19

Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Different modulation schemes: 4, 16, 32, 64 and 256-QAM
- Digital demodulator and square root raised cosine Nyquist filter with roll-off of 15% or 20%
- High performance adaptive equalizer (no training sequence needed)
- Digital detectors for generation of required control voltages for carrier recovery, clock recovery and AGC
- Digital-to-analog converters and operational amplifiers allowing high flexibility for selection of the (PLL) loop time constants
- High maximum symbol rate (r_s) of 7 Msymbols/s
- Input format: Straight binary or 2's complement (up to 9 bits, TTL compatible)
- Output format: 8-bit wide bus (CMOS compatible)
- I^2C-bus interface to initialize and monitor the demodulator. When no I^2C-bus usage; 64-QAM, 20% roll-off factor in default mode
- 5 V peripheral and analog supply voltage
- 3.3 V core supply voltage
- Boundary scan test.

2 APPLICATION

Demodulation for digital cable TV and cable modem.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(core)}$	core supply voltage		3.00	3.30	3.60	V
V_{DDD}	digital peripheral supply voltage		4.75	5.00	5.25	V
V_{DDA}	analog supply voltage		4.75	5.00	5.25	V
$I_{DDD(core)}$	core supply current	$V_{DDD(core)}$ = 3.3 V; note 1	–	100	–	mA
I_{DDD}	digital peripheral supply current	V_{DDD} = 5 V; note 1	–	14	–	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; note 1	–	16	–	mA
r_s	symbol rate		–	–	7	Msym/s
IL	implementation loss	note 2	–	0.7	–	dB
α	Nyquist roll-off (programmable)		–	15 or 20	–	%
SNR_{lock}	signal-to-noise ratio for locking a 64-QAM constellation		21	–	–	dB
	signal-to-noise ratio for locking a 256-QAM constellation		27	–	–	dB

Notes

1. The supply currents are specified for the maximum symbol frequency.
2. The implementation loss (IL) of the demodulator is defined as the distance between the measured and theoretical BER curve as function of signal-to-noise ratio at a BER = 10^{-6} for a back-to-back measurement at the IF frequency. This performance depends on the chosen loop parameters (see *Application notes*).

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8046H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

5 BLOCK DIAGRAM

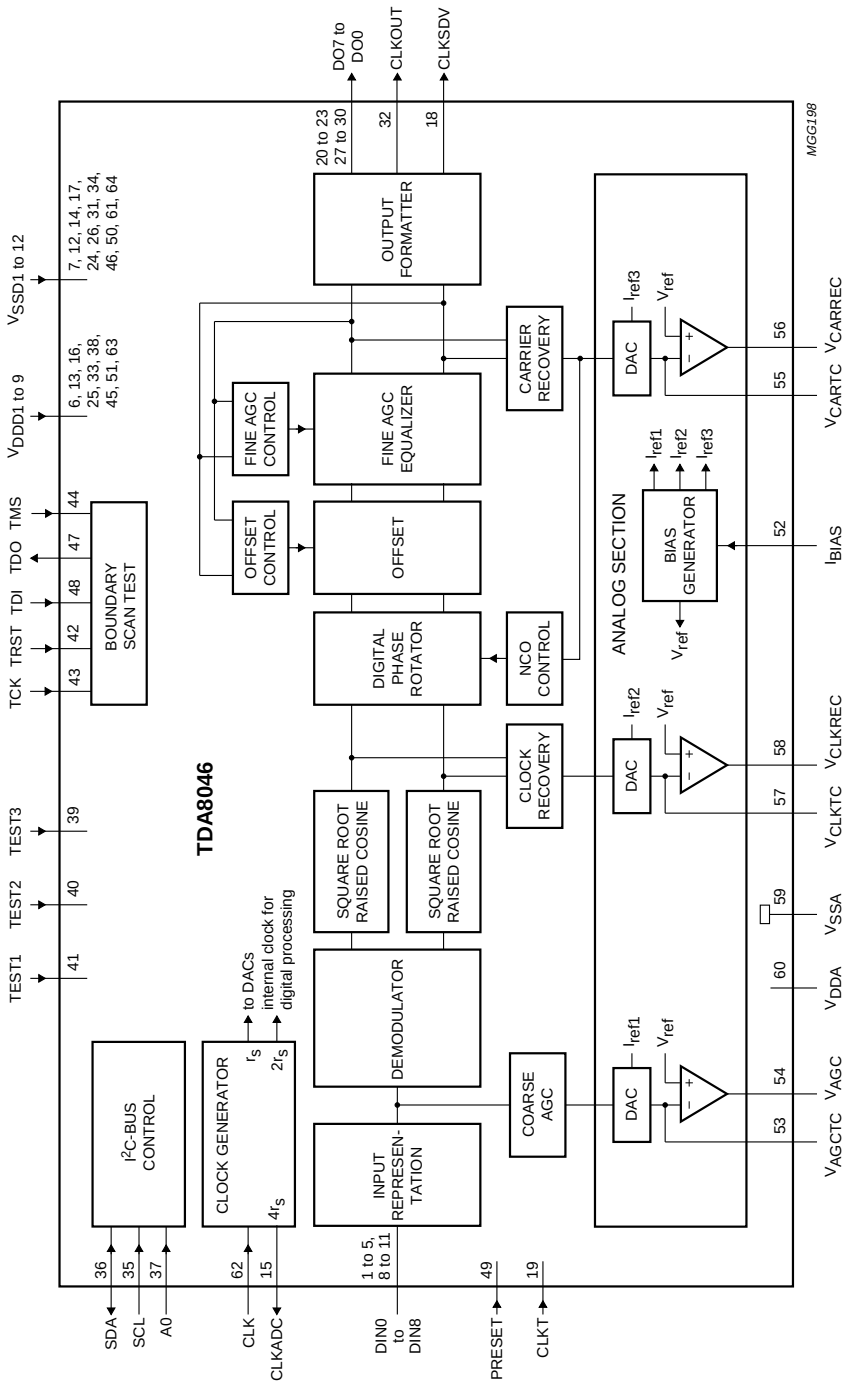


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DIN0	1	I	digital input bit 0 (LSB)
DIN1	2	I	digital input bit 1
DIN2	3	I	digital input bit 2
DIN3	4	I	digital input bit 3
DIN4	5	I	digital input bit 4
V_{DDD1}	6	supply	digital peripheral supply voltage 1 (+5 V)
V_{SSD1}	7	supply	digital ground 1; for input peripheral and core
DIN5	8	I	digital input bit 5
DIN6	9	I	digital input bit 6
DIN7	10	I	digital input bit 7
DIN8	11	I	digital input bit 8 (MSB)
V_{SSD2}	12	supply	digital ground 2; for core and clock buffers
V_{DDD2}	13	supply	digital supply voltage 2; for core and clock buffers (+3.3 V)
V_{SSD3}	14	supply	digital peripheral ground 3
CLKADC	15	O	clock output to ADC ($4 \times r_s$)
V_{DDD3}	16	supply	digital peripheral supply voltage 3 (+5 V)
V_{SSD4}	17	supply	digital ground 4; for core
CLKSDV	18	O	clock symbol data valid output
CLKT	19	I	for test purpose only
DO7	20	O	parallel data output (bit 7)
DO6	21	O	parallel data output (bit 6)
DO5	22	O	parallel data output (bit 5)
DO4	23	O	parallel data output (bit 4)
V_{SSD5}	24	supply	digital peripheral ground 5
V_{DDD4}	25	supply	digital peripheral supply voltage 4 (+5 V)
V_{SSD6}	26	supply	digital ground 6; for core
DO3	27	O	parallel data output (bit 3)
DO2	28	O	parallel data output (bit 2)
DO1	29	O	parallel data output (bit 1)
DO0	30	O	parallel data output (bit 0)
V_{SSD7}	31	supply	digital peripheral ground 7
CLKOUT	32	I	output formatter clock output
V_{DDD5}	33	supply	digital peripheral supply voltage 5 (+5 V)
V_{SSD8}	34	supply	digital peripheral ground 8
SCL	35	I	serial clock input (I^2C-bus)
SDA	36	I/O	serial data input/output (I^2C-bus)
A0	37	I	hardware address input (I^2C-bus)
V_{DDD6}	38	supply	digital peripheral supply voltage 6 (+5 V)
TEST3	39	I	test input 3 (normally connected to ground)
TEST2	40	I	test input 2 (normally connected to ground)

SYMBOL	PIN	I/O	DESCRIPTION
TEST1	41	I	test input 1 input (normally connected to ground)
TRST	42	I	optional asynchronous reset input
TCK	43	I	dedicated test clock input
TMS	44	I	input control signal
V_{DDD7}	45	supply	digital supply voltage 7; for core (+3.3 V)
V_{SSD9}	46	supply	digital ground 9; for core
TDO	47	O	serial test data output
TDI	48	I	serial test data input
PRESET	49	I	set device into default mode input
V_{SSD10}	50	supply	digital ground 10; for the digital section of the analog block
V_{DDD8}	51	supply	digital supply voltage 8; for the digital section of the analog block (+5 V)
I_{BIAS}	52	I	input bias current for DACs
V_{AGCTC}	53	O	inverted operational amplifier input voltage for loop filtering
V_{AGC}	54	O	analog output voltage for AGC
V_{CARTC}	55	O	inverted operational amplifier input voltage for carrier recovery loop filtering
V_{CARREC}	56	O	analog output voltage for carrier recovery
V_{CLKTC}	57	O	inverted operational amplifier input voltage for clock recovery loop filtering
V_{CLKREC}	58	O	analog output voltage for clock recovery
V_{SSA}	59	supply	analog ground
V_{DDA}	60	supply	analog supply voltage (+5 V)
V_{SSD11}	61	supply	digital ground 11; for clock
CLK	62	I	clock input ($4 \times r_s$)
V_{DDD9}	63	supply	digital supply voltage 9; for clock
V_{SSD12}	64	supply	digital peripheral ground 12

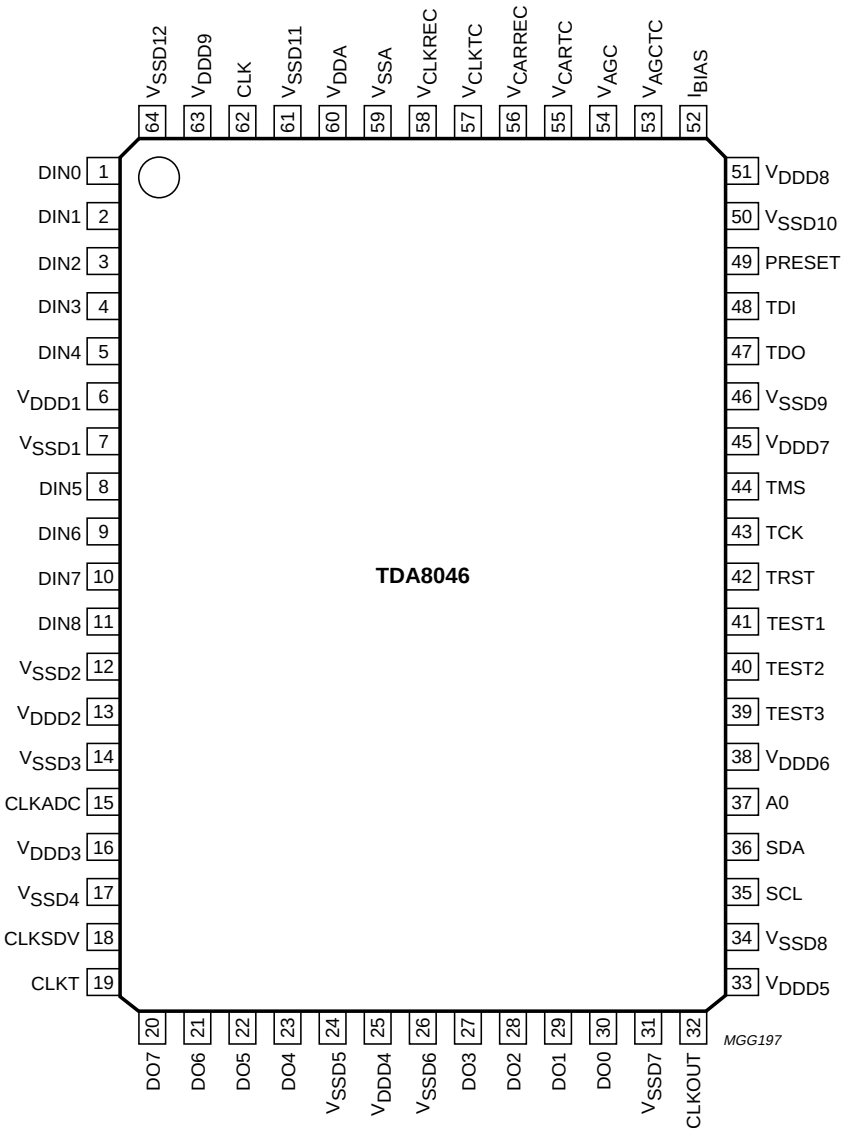


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

Figure 3 shows the application of the TDA8046 multi-mode QAM demodulator. The frequency of the IF signal (IF_{QAM}) is down converted to a frequency that equals the symbol rate (r_s) by a mixer which is driven from a local oscillator with a frequency of $f_{CAR} = f_{IF} + r_s$. After low pass filtering this baseband signal is applied to an external 8 or 9-bit ADC.

For 256-QAM, a 9-bit ADC is preferred, for the other modes an 8-bit ADC is sufficient.

The multi-mode QAM demodulator has digital detectors for AGC, carrier recovery and clock recovery. The on-chip DACs translate the detector values to analog control currents which are then integrated by a loop filter. To perform this loop filtering, an operational amplifier is integrated after each DAC.

The carrier recovery consists of a two-loop system. The outer loop is shown in Fig.3, and controls both phase and frequency at a low speed. The inner loop controls the carrier phase at a high speed (wide loop bandwidth).

The AGC also consists of two loops; the outer loop is the coarse AGC and one inner loop is the fine AGC.

The recovered symbols are converted into bits according to a demapping scheme and represented at the output in an 8-bit parallel output format. The QAM demodulator can be initialized and monitored by the I²C-bus interface.

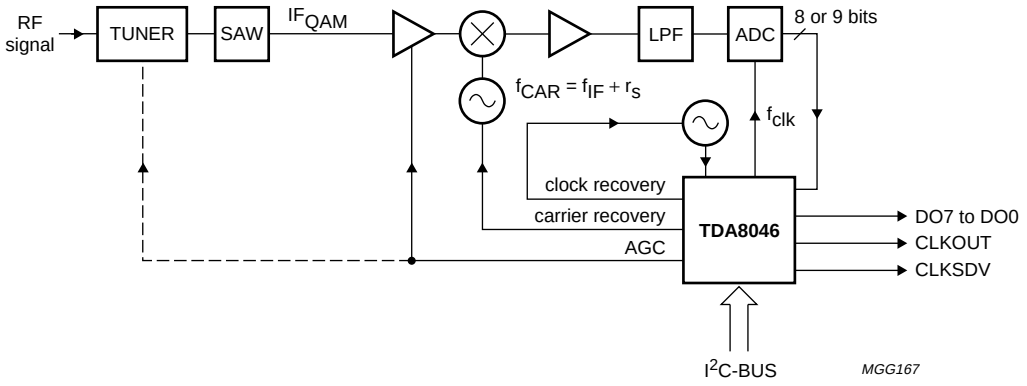


Fig.3 Application with multi-mode QAM demodulator.

7.1 Functional description of the individual blocks

The functional block diagram of the multi-mode QAM demodulator is illustrated in Fig.1. This section describes the individual blocks in the demodulator. After adaptation for the used input format (2's complement or binary), the input signal is demodulated in the I and Q baseband signals which are applied to the inputs of the half-Nyquist filter (equals square root raised cosine). To avoid overloading of the ADC, an AGC detector is placed after the adaptation for the input format. The control value for the clock recovery is generated after half Nyquist filtering. The echoes created in the cable network are reduced significantly in the equalizer.

The equalizer produces a 'clean' constellation diagram from which the information for the carrier recovery is derived. This constellation is also applied to the output formatter which demaps the transmitted symbols in corresponding bits. The carrier recovery and lock detection functions are based on the equalizer output. The output of the equalizer is applied to an output formatter, which translates the symbol bits to a FEC input format. The digital outputs of the clock recovery, AGC, and carrier recovery section are converted into currents which are integrated by the loop filters.
To make these loop filters active, operational amplifiers are integrated on the chip.

The TDA8046 can handle five different digital modulation schemes; 4, 16, 32, 64 and 256-QAM. These schemes are selectable via the I^{2}C-bus interface.

7.1.1 Quadrature demodulator and half Nyquist filter

Quadrature demodulation is accomplished after selection of the appropriate input format via the I^{2}C-bus.
The in-phase and quadrature components are both applied to a half Nyquist filter. In default mode, this filter gives a 20% roll-off half Nyquist shaping. The basic schematic of the quadrature demodulator followed by the half Nyquist filter is shown in Fig.4. The signs of the multiplication factors in the Q-branch can be inverted (I^{2}C-bus bit INVD).

When using an 8-bit ADC the LSB of the 9-bit input word should be connected to the positive supply (V_{DDD}). This ensures a symmetrical 2's complement representation which can be multiplied by −1 in a correct (2's complement) way. The overall transfer function of the square root raised cosine filters is shown in Figs 5 and 6.

For characteristics see Chapter 10.

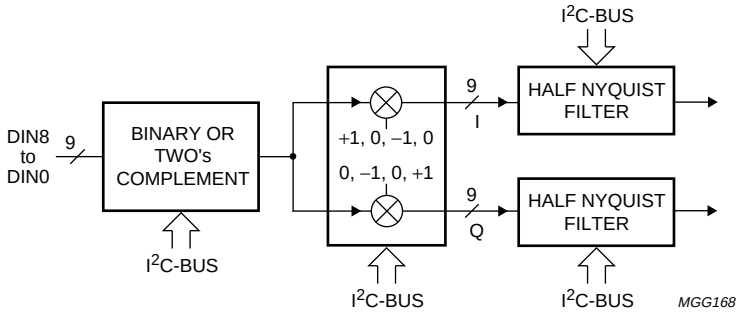


Fig.4 Schematic diagram of the quadrature demodulator and half Nyquist filter.

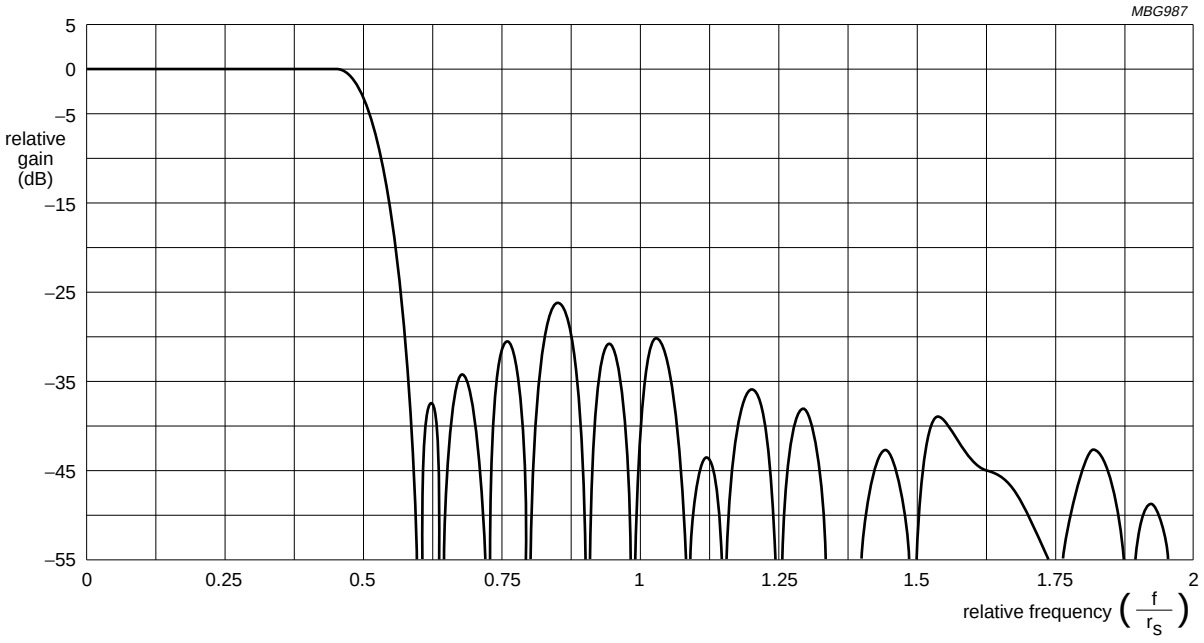


Fig.5 Half Nyquist receiver filter transfer function (20% roll-off).

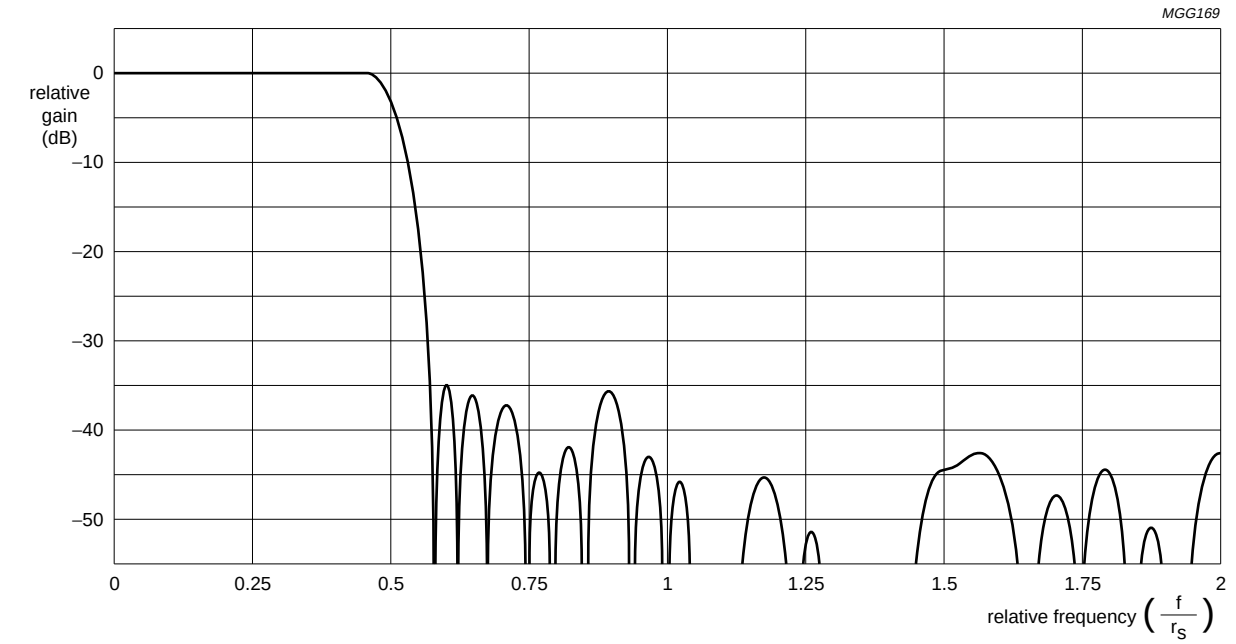


Fig.6 Half Nyquist receiver filter transfer function (15% roll-off).

7.1.2 EQUALIZER

This function is realized with a T spaced 12 or 14 taps (selected via the I²C-bus) adaptive filter with a feedback part. The equaliser is based on a Decision Feedback Equalizer (DFE) structure with Least Mean Square (LMS) coefficient updating algorithm. No training sequence is required. The block schematic of the total equalizer is shown in Fig.8. The main tap of the equalizer is adjustable for fine AGC function (6 dB AGC range). The settings of the equalizer taps can be read via the I²C-bus. If the equalizer diverges, an alarm bit is set (I²C-bus bit ALEQ) and an automatic reset of the taps can be performed (I²C-bus bit EAR).

To improve acquisition time, the convergence steps of the FFE/DFE parts of the equalizer are programmable via the I²C-bus. When the system locks, the steps are automatically modified for optimum performances.

Besides reading the equalizer tap values, the main tap of the equalizer can also be programmed. After setting the main tap, the other coefficients can be set to zero.
The equalizer settings can also be frozen via the I²C-bus.

The equalizer has been proven to work correctly under bad channel conditions as indicated in Table 1. It is guaranteed that all loops (including equalizer) converge at a SNR of 21 dB for a 64-QAM modulation format and 27 dB for a 256-QAM modulation format.

Table 1 Channel echo profile

DELAY	AMPLITUDE	PHASE
$\frac{3}{8} \times T_{sym}$	0.08	130°
$1\frac{1}{8} \times T_{sym}$	0.20	60°
$2 \times T_{sym}$	0.05	310°
$4\frac{5}{8} \times T_{sym}$	0.10	200°
$6\frac{7}{8} \times T_{sym}$	0.03	200°

Figure 7 represents the QAM spectrum seen by the equalizer. It corresponds (in the frequency domain) to the multiplication of a full nyquist spectrum by the impulse response of the channel specified in Table 1.

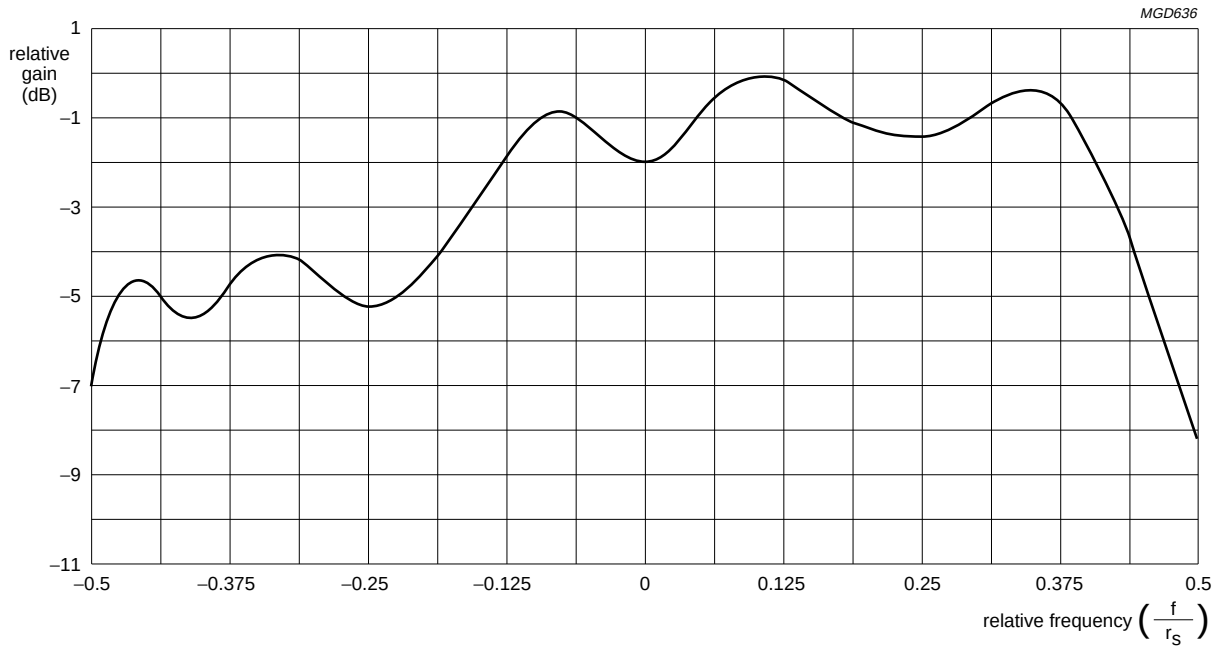


Fig.7 QAM spectrum with echo profile as seen by the equalizer.

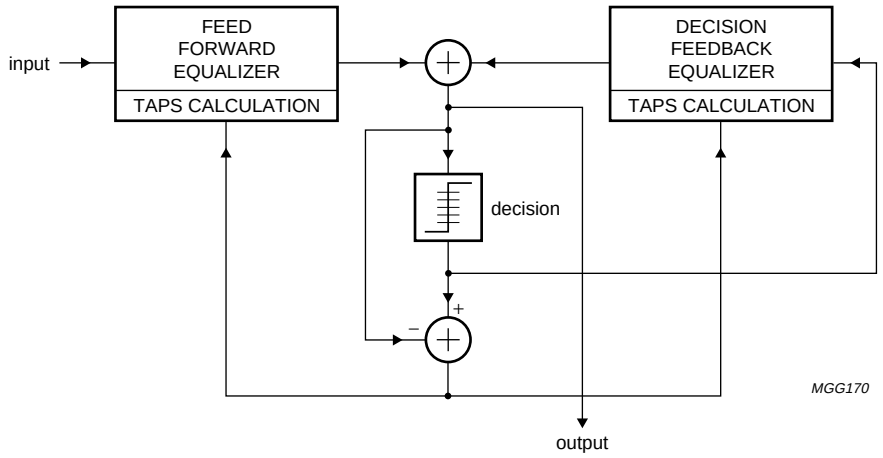


Fig.8 DFE equalizer structure.

7.1.3 LOCK DETECTOR

The lock detector indicates whether all algorithms in the demodulator are converged or not. For a symbol error rate (at the input of the demodulator) smaller than 2×10^{-2}, the detector will give the indication 'LOCK' (I^2C-bus bit LK = 1). For larger symbol error rates, the detector will generate the 'UNLOCK' signal (I^2C-bus bit LK = 0).
It should ne noted that this 'UNLOCK' signal is generated before any other part of the demodulator loses lock.
The lock detector is part of the carrier recovery loop, see Fig.9. The Lock Detector Threshold (LDT) can be changed with the help of the I^2C-bus. The estimation algorithm used in the lock detector also provides information about the SER ratio which can be read out via the I^2C-bus interface.

For characteristics see Chapter 11.

7.1.4 CARRIER RECOVERY

The carrier recovery detector consists of a Phase-Frequency Detector (PFD) and Phase Detector (PD). Depending on the mode of operation, the carrier recovery is switched either between the phase frequency (no lock) or the phase detector (lock). The carrier recovery consists of the following two loops:

1. The outer loop; this loop controls the phase and frequency of the incoming QAM signal at the IF frequency in such a way that the constellation is optimally positioned for detection.
2. The inner loop; the bandwidth of this loop can be large and can therefore reduce the influence of large bandwidth phase noise.

A fully digital carrier recovery function is also possible and can be selected via the I^2C-bus. Should this configuration be used, then the external components of the loop filter will not have to be implemented.

Four different maximum DAC output currents can be selected via the I^2C-bus. The output currents of the DAC are defined in such a way that a VCO with a behaviour as shown in Fig.9 can be connected directly to the output of the integrated operational amplifier. Should the VCO slope be negative then the sign of the current can be inverted by the I^2C-bus. Figure 10 defines the DAC output currents.

For characteristics see Chapter 12.

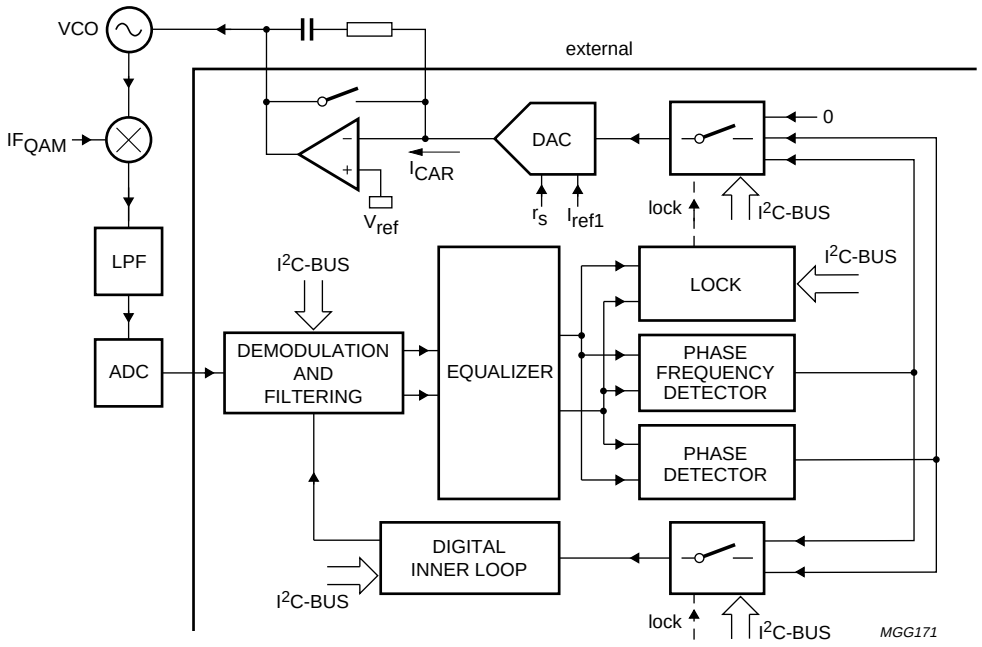
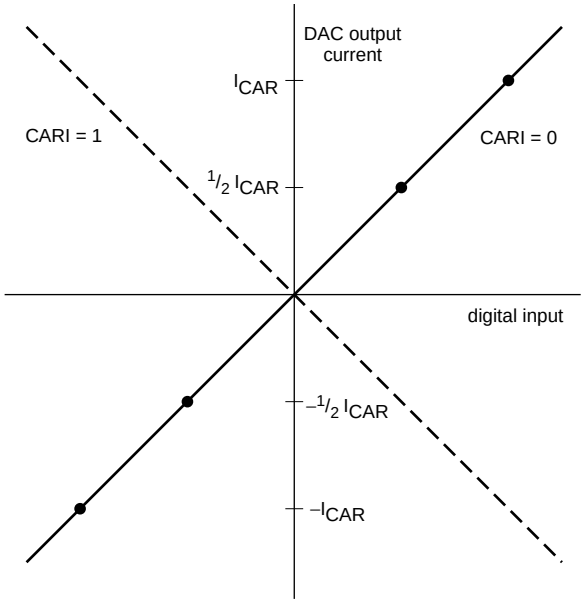
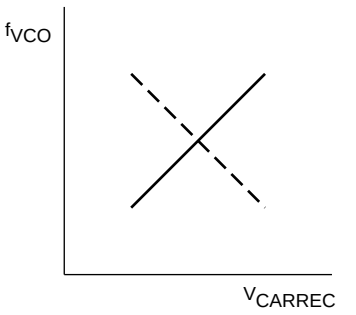


Fig.9 Schematic diagram of the carrier recovery.





MGG180

I_{pos} = positive output current.
I_{neg} = negative output current.

$$I_O = \frac{(I_{pos} - I_{neg})}{2}$$

$$\Delta I_O = \frac{(I_{pos} + I_{neg})}{(I_{pos} - I_{neg})} \times 100$$

Fig.10 Definition of the DAC currents and the expected frequency behaviour of the VCO.

7.1.5 CLOCK RECOVERY

The clock recovery function uses the unequalized I and Q signals, i.e. the half Nyquist filter outputs (see Fig.4). The clock recovery section generates a control value each symbol period. As this algorithm is based on the energy maximization, both main and mid symbols are required at the input. Consequently, the input data rate is twice the symbol rate. The schematic diagram of this detector is illustrated in Fig.11.

The clock generator generates the required internal clocks from the VCXO clock signal at $4 \times r_s$. The input stage amplifier of this generator enables the designer to supply a low amplitude oscillator signal to the TDA8046. The DAC output current range (I_{CLK}) can be varied via the I^2C-bus. The sign of the output current can also be inverted to adjust for the correct sign of the VCXO slope.

For characteristics see Chapter 13.

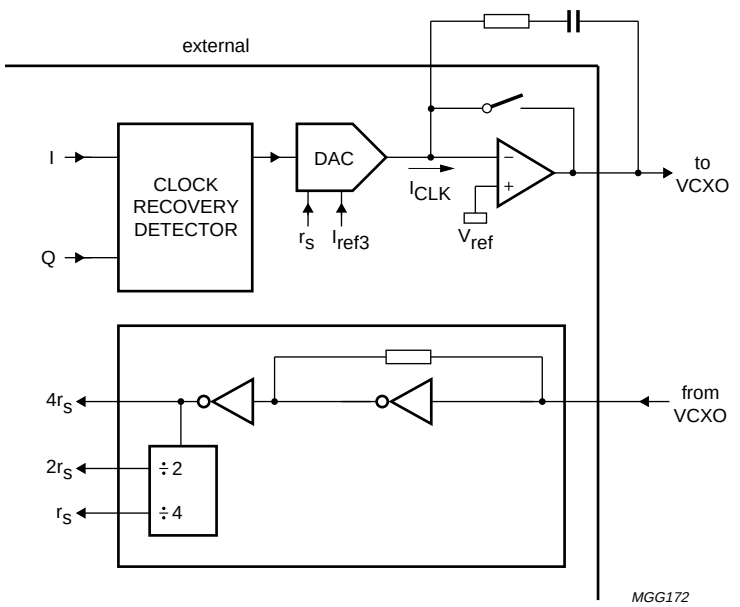
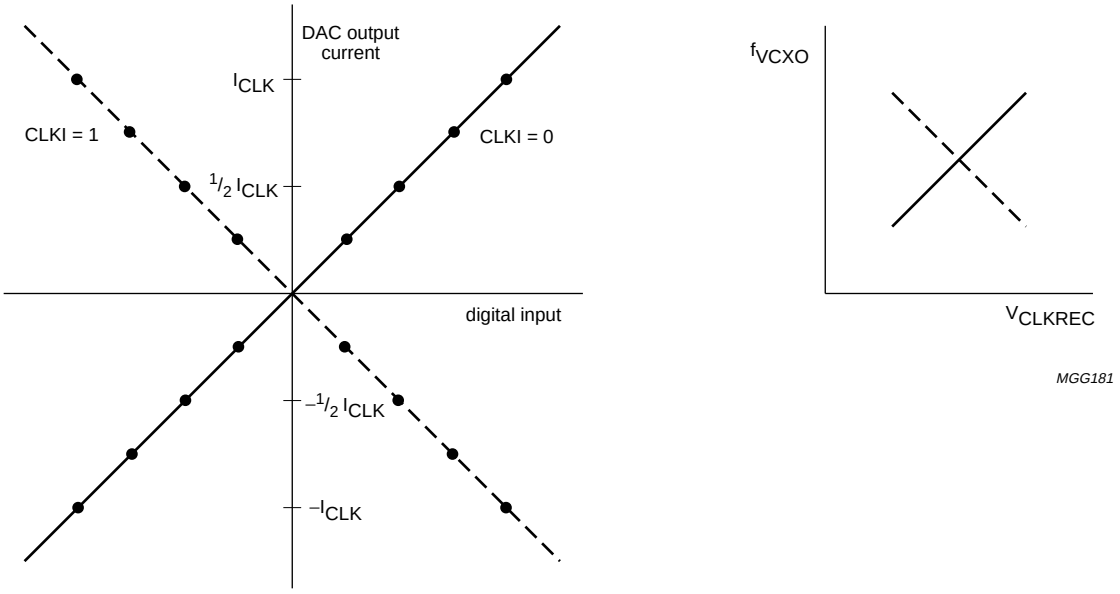


Fig.11 Schematic diagram of the clock recovery.



I_{pos} = positive output current; I_{CLK}.
I_{neg} = negative output current; $-I_{CLK}$.

$$I_{oCLK} = \frac{(I_{pos} - I_{neg})}{2}$$

$$\Delta I_{oCLK} = \frac{(I_{pos} + I_{neg})}{(I_{pos} - I_{neg})} \times 100$$

Fig.12 The definition of the DAC currents and the expected frequency behaviour of the VCXO for clock recovery.

7.1.6 AGC

The AGC estimates the mean power based on the digital input signal and relates this to a peak value for a given constellation. To avoid overloading of the ADC, this estimation of the peak signals is used to control the AGC loop. The implemented AGC covers a range of ±20 dB in gain variance. A schematic diagram of the AGC is illustrated in Fig.13.

If the SAW filter does not have sufficient adjacent channel attenuation, the AGC threshold can be varied to avoid clipping of the ADC. To do this, the threshold is made programmable via the I²C-bus (byte ATH). Table 2 shows that for each mode, a new ATH value (on address 08) must be set with the help of the I²C-bus.

The I²C-bus data on address 08 is a factor 16 smaller than the used AGC threshold ATH.

The DAC output current range can be varied via the I²C-bus interface (bits AGCA and AGCB) and the sign of the current can be inverted (bit AGCI). The definition of the DAC currents and the expected frequency behaviour of the AGC is illustrated in Fig.14.

For characteristics see Chapter 14.

Table 2 AGC threshold values

MODE	ATH (AGC THRESHOLD)	I²C-BUS DATA FOR ADDRESS 08
256, 64, 16 and 4-QAM	2040	7F
32-QAM	1442	5A

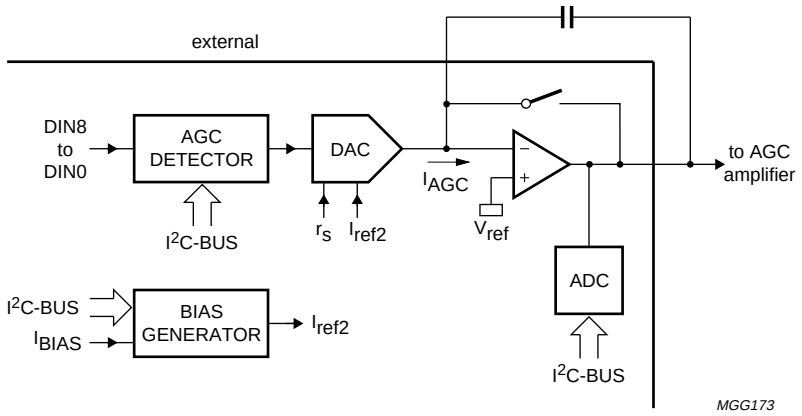
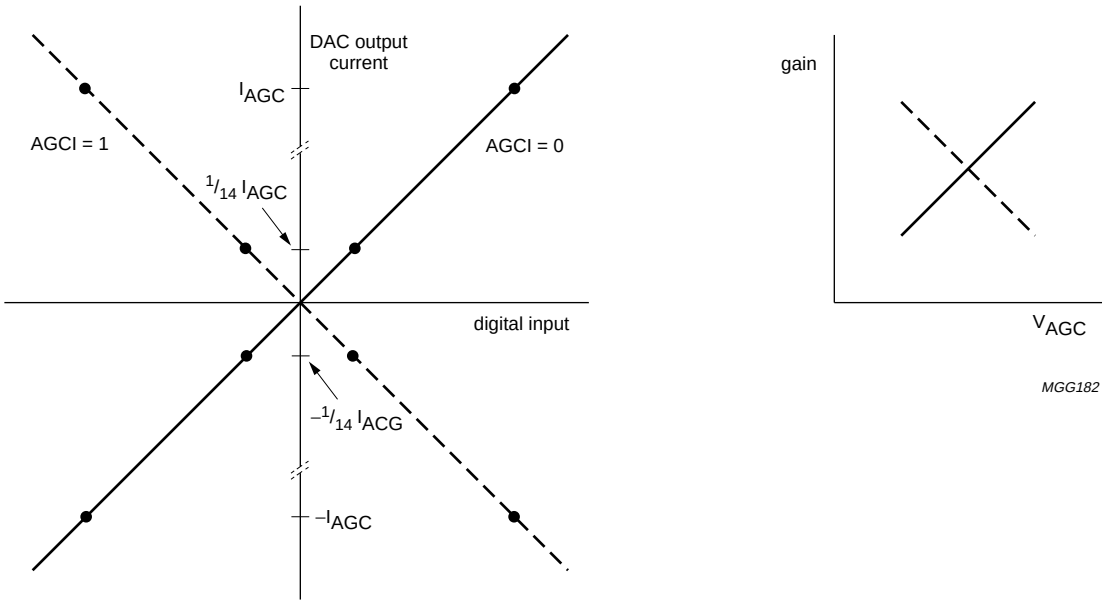


Fig.13 AGC schematic diagram.



I_{pos} = positive output current; I_{CLK}.
I_{neg} = negative output current; $-I_{CLK}$.

$$I_{oAGC} = \frac{(I_{pos} - I_{neg})}{2}$$

$$\Delta I_{oAGC} = \frac{(I_{pos} + I_{neg})}{(I_{pos} - I_{neg})} \times 100$$

Fig.14 Definition of the DAC currents and the expected frequency behaviour of the AGC.

7.1.7 Offset control

To compensate offsets in the I and Q branch, due to spurious signals at the symbol frequency at the ADC input, an offset compensation loop is included. This loop forces the constellation to be symmetrically distributed over its four quadrants. This function can be switched off by I²C-bus bit OFFS.

7.1.8 Loop amplifiers

Analog switches are integrated to discharge the loop filter capacitors or for test purposes on application boards (a reference voltage equal to the half of the positive supply voltage V_{DDA} is available at the output of the amplifier when the switches are closed). The I²C-bus bit ANAS controls the three switches simultaneously. A schematic diagram of the loop amplifier and analog switch is illustrated in Fig.15.

For characteristics see Chapter 15.

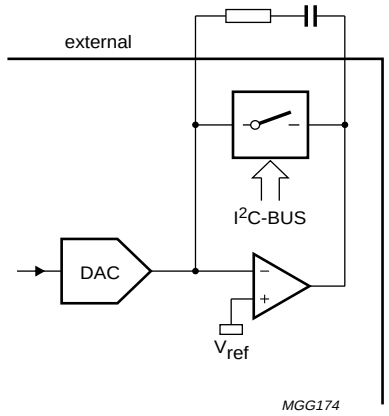


Fig.15 Loop amplifier and analog switch.

7.1.9 Output formatter

The output formatter transforms the detected symbols into bits in accordance with the selected mapping. The TDA8046 has four possible mapping formats which can be selected via the I²C-bus interface. The demapping procedure and the corresponding bits are defined in Fig.16. After demapping the bits are allocated to the output. This output allocation corresponds to one of the selected demapping schemes.

By using the I²C-bus, it is possible to obtain the following output formats:

- 8 bits parallel
- semi-serial
- I and Q 8 bits multiplexed.

The implemented demapping formats and output bit allocation are illustrated in Figs 17 to 30.

7.1.10 Boundary scan

The TDA8046H offers the possibility of boundary scan test. The IEEE Standard Test Access Port and Boundary Scan Architecture allows board manufacturers to test board interconnections by using the boundary scan functions.

Complete information on boundary scan test is available in *“Application note AN96048”*.

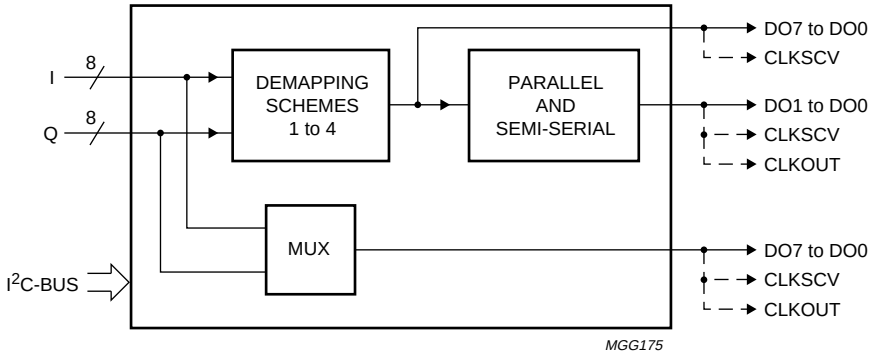
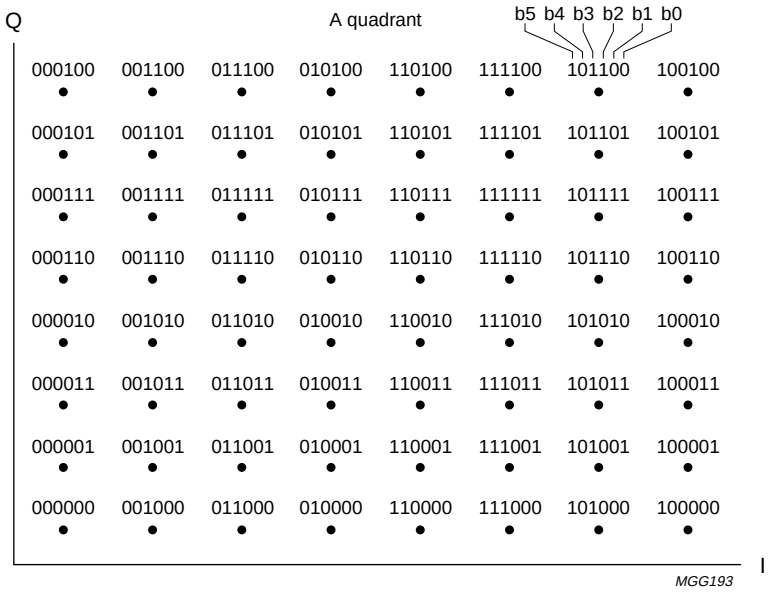


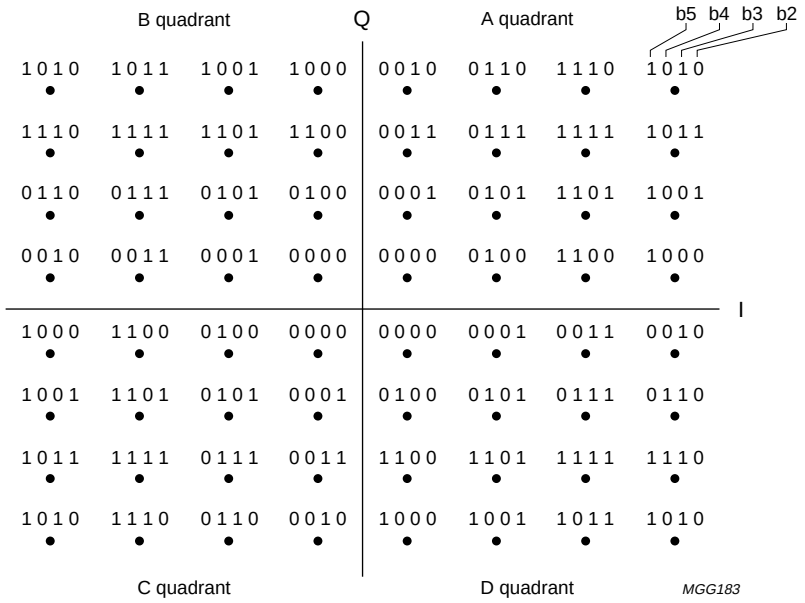
Fig.16 Schematic diagram of the output formatter.

7.1.10.1 Demapping scheme 1; differential decoding



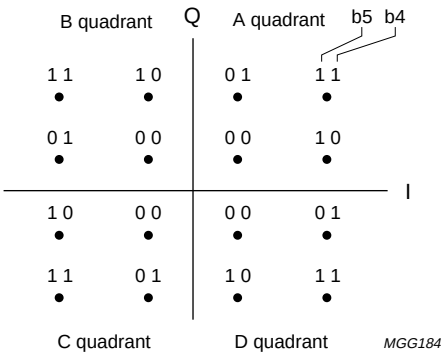
Bit allocation for 256-QAM: b5, b4, b3, b2, b1 = b0 = 0; b7 and b6 differentially decoded (see Table 3).

Fig.17 Demapping scheme 1; bit allocation: 256-QAM.



Bit allocation for 4-QAM: b5 = b4 = b3 = b2 = b1 = b0 = 0; b7 and b6 differentially decoded (see Table 3).
Bit allocation for 64-QAM: b5, b4, b3 and b2; b0 = b1 = 0; b7 and b6 differentially decoded (see Table 3).

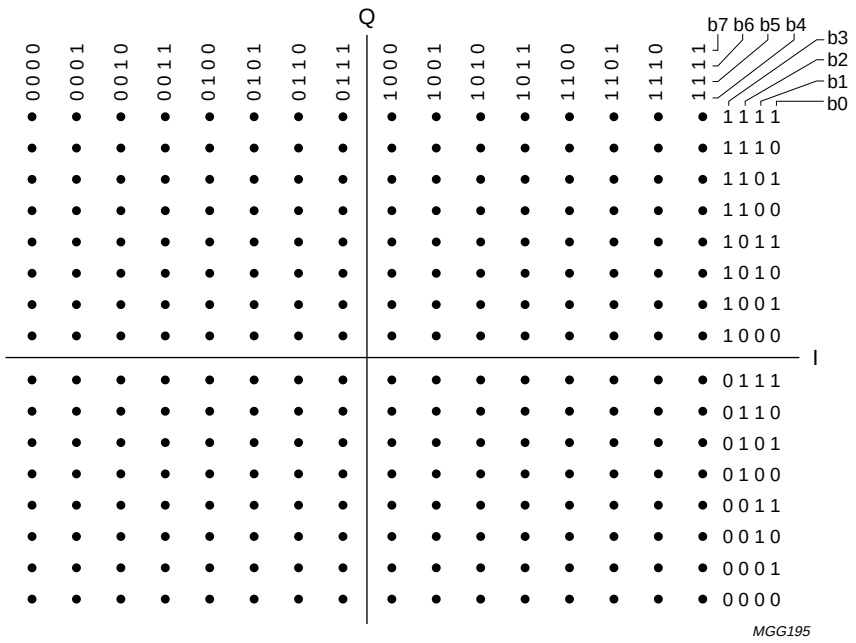
Fig.18 Demapping scheme 1; bit allocation: 4-QAM and 64-QAM.



Bit allocation for 16-QAM: b5 and b4; b3 = b2 = b1 = b0 = 0; b7 and b6 differentially decoded (see Table 3).
Bit allocation for 32-QAM: not implemented.

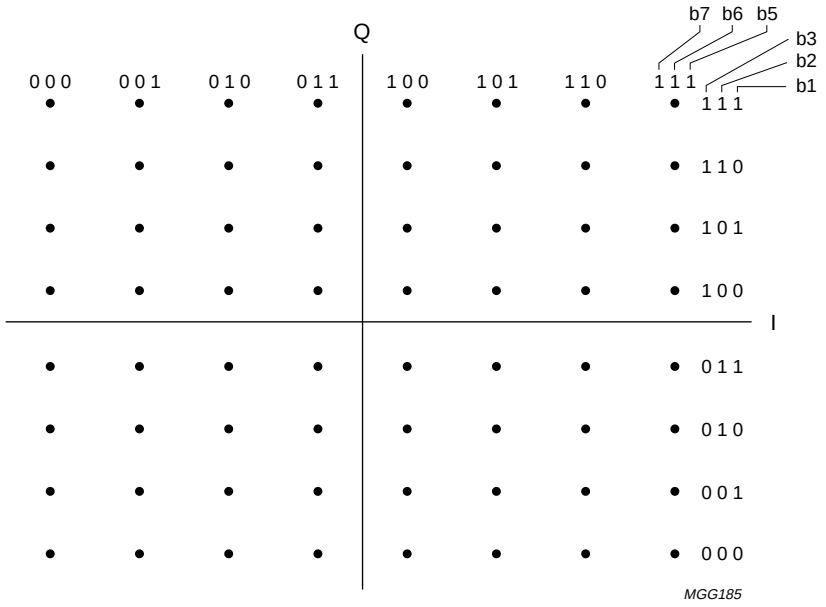
Fig.19 Demapping scheme 1; bit allocation: 16-QAM and 32-QAM.

7.1.10.2 Demapping scheme 2; direct translation



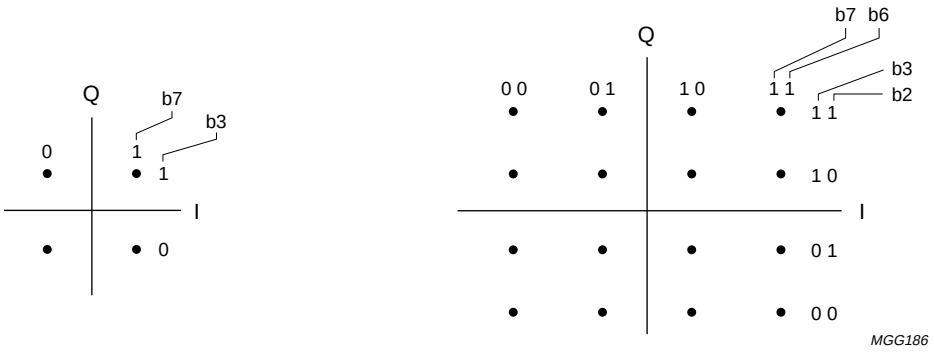
Bit allocation for 256-QAM: b7, b6, b5, b4, b3, b2, b1, b0.

Fig.20 Demapping scheme 2; bit allocation: 256-QAM.



Bit allocation for 64-QAM: b7, b6, b5, b3, b2, b1; b4 = b0 = 0.
Bit allocation for 32-QAM: not implemented.

Fig.21 Demapping scheme 2; bit allocation: 64-QAM and 32-QAM.

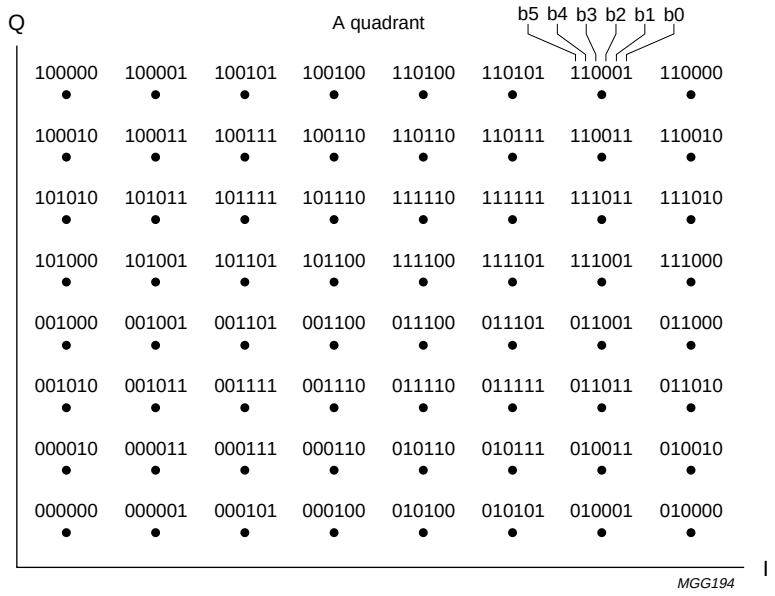


a. Bit allocation for 4-QAM: b7 and b3; b6 = b5 = b4 = b2 = b1 = b0 = 0.

b. Bit allocation for 16-QAM: b7, b6, b3 and b2; b5 = b4 = b1 = b0 = 0.

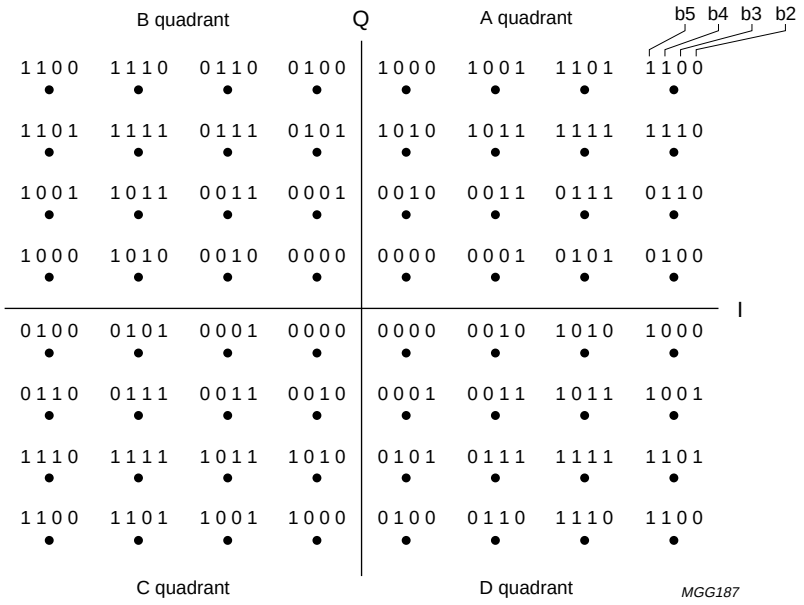
Fig.22 Demapping scheme 2; bit allocation: 4-QAM and 16-QAM.

7.1.10.3 Demapping scheme 3; differential decoding: Draft prETS 429: 1994



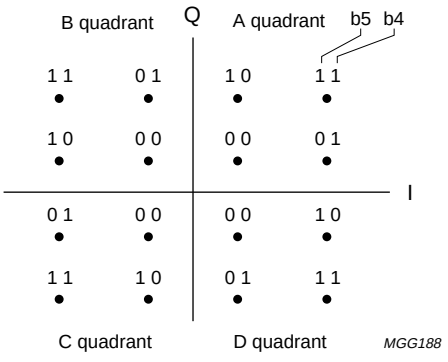
Bit allocation for 256-QAM: b5, b4, b3, b2, b1, b0; b7 and b6 differentially decoded (see Table 3).

Fig.23 Demapping scheme 3; bit allocation: 256-QAM.



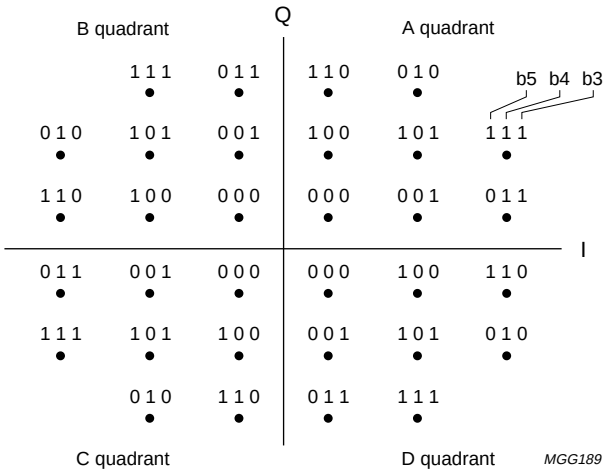
Bit allocation for 4-QAM: b5 = b4 = b3 = b2 = b1 = b0 = 0; b7 and b6 differentially decoded (see Table 3).
Bit allocation for 64-QAM: b5, b4, b3 and b2; b1 = b0 = 0; b7 and b6 differentially decoded (see Table 3).

Fig.24 Demapping scheme 3; bit allocation: 4-QAM and 64-QAM.



Bit allocation for 16-QAM: b5 and b4; b3 = b2 = b1 = b0 = 0; b7 and b6 differentially decoded (see Table 3).

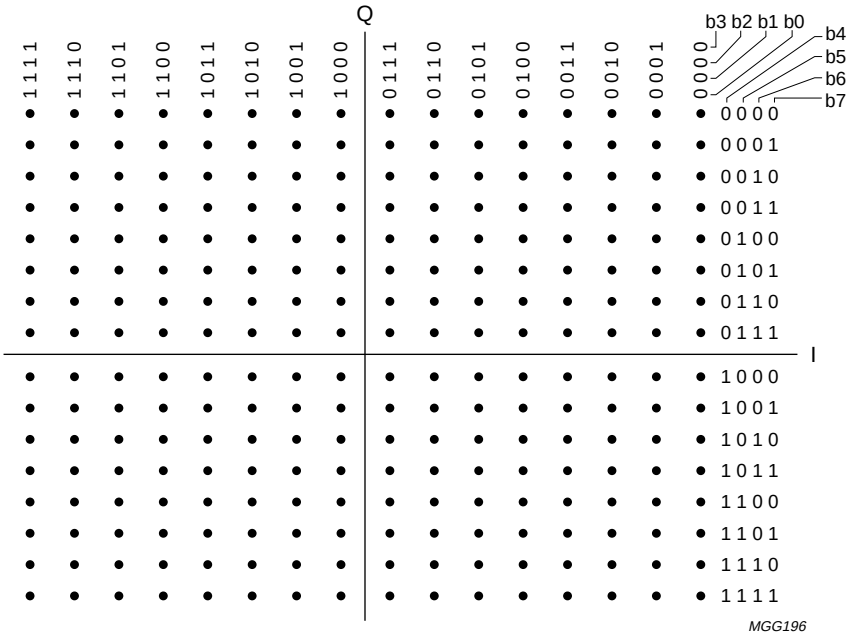
Fig.25 Demapping scheme 3; bit allocation: 16-QAM.



Bit allocation for 32-QAM: b5, b4 and b3; b2 = b1 = b0 = 0; b7 and b6 differentially decoded (see Table 3).

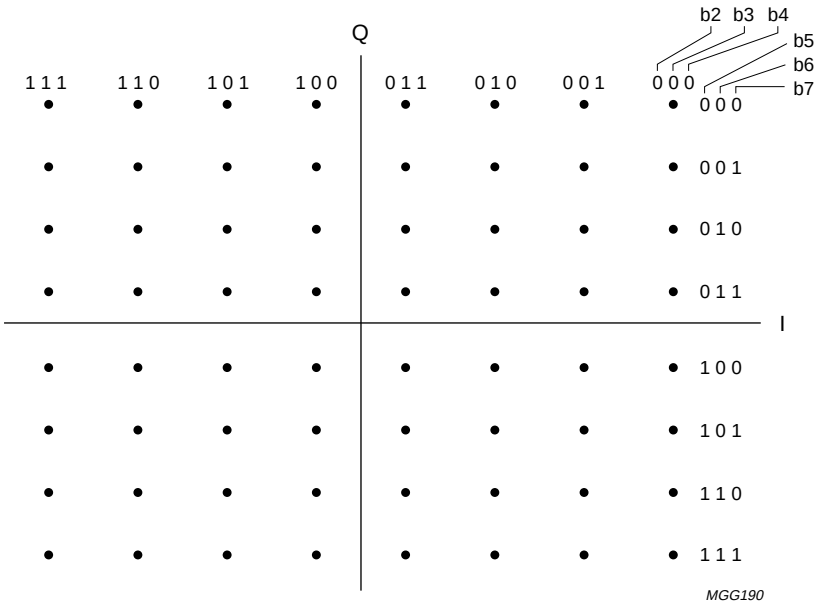
Fig.26 Demapping scheme 3; bit allocation: 32-QAM.

7.1.10.4 Demapping scheme 4; direct translation: HP8782B/K03



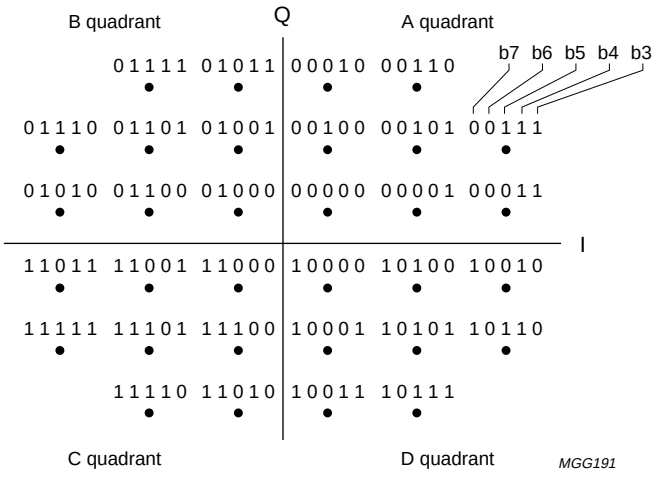
Bit allocation for 256-QAM: b7, b6, b5, b4, b3, b2, b1, b0.

Fig.27 Demapping scheme 4; bit allocation: 256-QAM.



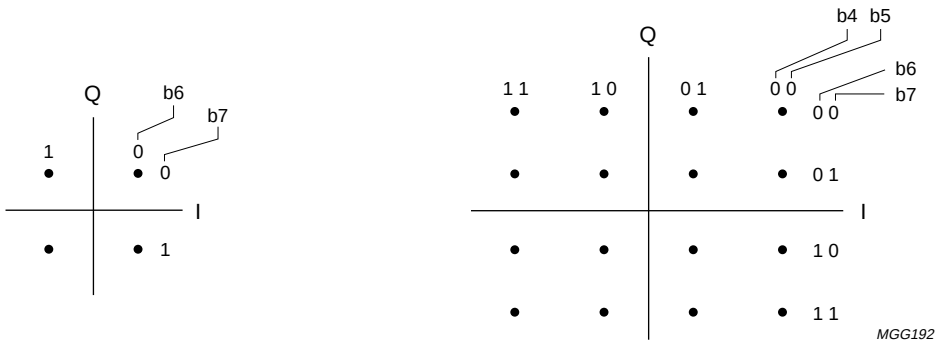
Bit allocation for 64-QAM: b7, b6, b5, b4, b3 and b2; b1 = b0 = 0.

Fig.28 Demapping scheme 4; bit allocation: 64-QAM.



Bit allocation for 32-QAM: b7, b6, b5, b4 and b3; b2 = b1 = b0 = 0.

Fig.29 Demapping scheme 4; bit allocation: 32-QAM.



a. Bit allocation for 4-QAM: b7 and b6; b5 = b4 = b3 = b2 = b1 = b0 = 0. b. Bit allocation for 16-QAM: b7, b6, b5 and b4; b3 = b2 = b1 = b0 = 0.

Fig.30 Demapping scheme 4; bit allocation: 4-QAM and 16-QAM.

Table 3 Definition of two MSB's in modulation schemes 1 and 3

QUADRANT OF CURRENTLY RECEIVED SYMBOL	QUADRANT OF PREVIOUSLY RECEIVED SYMBOL	PHASE CHANGE (DEGREES)	CURRENT OUTPUT BITS			
			SCHEME 1		SCHEME 3	
			b7	b6	b7	b6
A	A	0	0	0	0	0
A	B	270	1	0	0	1
A	C	180	1	1	1	1
A	D	90	0	1	1	0
B	A	90	0	1	1	0
B	B	0	0	0	0	0
B	C	270	1	0	0	1
B	D	180	1	1	1	1
C	A	180	1	1	1	1
C	B	90	0	1	1	0
C	C	0	0	0	0	0
C	D	270	1	0	0	1
D	A	270	1	0	0	1
D	B	180	1	1	1	1
D	C	90	0	1	1	0
D	D	0	0	0	0	0

Tables 4 and 5 give the output format of the data for semi-serial mode operations.

Table 4 Semi-serial format 256, 64 and 32-QAM; see note 1

SLOT	256-QAM			64-QAM			32-QAM		
	DO1	DO0	CLKSDV	DO1	DO0	CLKSDV	DO1	DO0	CLKSDV
0	$S_{n-1}(7)$	$S_{n-1}(6)$	1	$S_{n-1}(5)$	$S_{n-1}(4)$	1	$S_{n-1}(4)$	$S_{n-1}(3)$	1
1	$S_{n-1}(5)$	$S_{n-1}(4)$	1	$S_{n-1}(3)$	$S_{n-1}(2)$	1	$S_{n-1}(2)$	$S_{n-1}(1)$	1
2	$S_{n-1}(3)$	$S_{n-1}(2)$	1	$S_{n-1}(1)$	$S_{n-1}(0)$	1	X	X	0
3	$S_{n-1}(1)$	$S_{n-1}(0)$	1	X	X	0	X	X	0
4	$S_n(7)$	$S_n(6)$	1	$S_n(5)$	$S_n(4)$	1	$S_{n-1}(0)$	$S_n(4)$	1
5	$S_n(5)$	$S_n(4)$	1	$S_n(3)$	$S_n(2)$	1	$S_n(3)$	$S_n(2)$	1
6	$S_n(3)$	$S_n(2)$	1	$S_n(1)$	$S_n(0)$	1	$S_n(1)$	$S_n(0)$	1
7	$S_n(1)$	$S_n(0)$	1	X	X	0	X	X	0

Note

1. The semi-serial format is only valid for demapping schemes 1, 3 and 4.

Table 5 Semi-serial format 16-QAM and 4-QAM; see note 1

SLOT	16-QAM			4-QAM		
	DO1	DO0	CLKSDV	DO1	DO0	CLKSDV
0	$S_{n-1}(3)$	$S_{n-1}(2)$	1	$S_{n-1}(1)$	$S_{n-1}(0)$	1
1	$S_{n-1}(1)$	$S_{n-1}(0)$	1	X	X	0
2	X	X	0	X	X	0
3	X	X	0	X	X	0
4	$S_n(3)$	$S_n(2)$	1	$S_n(1)$	$S_n(0)$	1
5	$S_n(1)$	$S_n(0)$	1	X	X	0
6	X	X	0	X	X	0
7	X	X	0	X	X	0

Note

1. The semi-serial format is only valid for demapping schemes 1, 3 and 4.

7.1.11 I²C-BUS INTERFACE

The TDA8046 is controlled by an I²C-bus. For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting READ or WRITE mode. It should be noted that the TDA8046 starts up in accordance with to the settings defined in Tables 7, 8 and 9.

Table 6 Slave address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	0	0	1	1	1	A0	X

Table 7 WRITE (R/$\overline{W}$ = 0)

FUNCTION	ADD	D7	D6	D5	D4	D3	D2	D1	D0
DAC current inversion/general	00	AGCI	CLKI	CARI	OUTE	DEM	NYQ	DPHR	RST
Demodulator	01	INP	RLF	OUTB	OUTA	INVD	CONC	CONB	CONA
DAC/OFFS/switch	02	ANAS	OFFS	AGCB	AGCA	CLKB	CLKA	CARB	CARA
Digital test/output formatter	03	–	–	–	–	OUTF	TSEL2	TSEL1	TSEL0
Digital loop filter B.W.	04	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA1	DCA0
Digital loop filter B.W.	05	FSOL	–	–	–	–	DCB2	DCB1	DCB0
Lock detector threshold	06	LDT7	LDT6	LDT5	LDT4	LDT3	LDT2	LDT1	LDT0
Lock detector window size	07	–	–	–	–	–	–	WS1	WS0
AGC detector threshold	08	ATH7	ATH6	ATH5	ATH4	ATH3	ATH2	ATH1	ATH0
Equalizer mode	09	–	–	EAR	FFEL	EDFE	EFFE	EFC	PRESET
Equalizer tap FFEI	0A	FFEI07	FFEI06	FFEI05	FFEI04	FFEI03	FFEI02	FFEI01	FFEI00
Equalizer steps	0B	–	FSTP2	FSTP1	FSTP0	–	DSTP2	DSTP1	DSTP0

Table 8 Default settings after reset

FUNCTION	ADD	D7	D6	D5	D4	D3	D2	D1	D0
DAC current inversion/ general	00	0	1	0	1	1	1	0	0
Demodulator	01	1	1	0	0	0	0	1	1
DAC/OFFS/switch	02	0	1	0	1	0	1	0	1
Digital test/output formatter	03	–	–	–	–	0	0	0	0
Digital loop filter B.W.	04	0	1	0	0	0	0	0	0
Digital loop filter B.W.	05	1	–	–	–	–	1	0	0
Lock detector threshold	06	0	0	0	1	1	0	0	0
Lock detector window size	07	–	–	–	–	–	–	0	0
AGC detector threshold	08	0	1	1	1	1	1	1	1
Equalizer mode	09	–	–	0	1	0	0	0	0
Equalizer tap FFEI	0A	0	1	0	0	0	0	0	0
Equalizer steps	0B	–	0	0	0	–	0	0	0

Table 9 READ ($R/\overline{W}$ = 1)

FUNCTION	ADD	D7	D6	D5	D4	D3	D2	D1	D0
V_{CARREC} (4 bits)	00	–	–	–	–	CR03	CR02	CR01	CR00
V_{CLKREC} (4 bits)	01	–	–	–	–	CL03	CL02	CL01	CL00
V_{AGC} (4 bits)	02	–	–	–	–	AG03	AG02	AG01	AG00
Alarm equalizer/ lock detector	03	–	–	–	ALEQ	–	–	–	LK
SER estimation	04	LE7	LE6	LE5	LE4	LE3	LE2	LE1	LE0
FFEI3	05	b7	b6	b5	b4	b3	b2	b1	b0
....	...	b7	b6	b5	b4	b3	b2	b1	b0
FFEI0	08	b7	b6	b5	b4	b3	b2	b1	b0
DFEI1	09	b7	b6	b5	b4	b3	b2	b1	b0
....	...	b7	b6	b5	b4	b3	b2	b1	b0
DFEI7	0F	b7	b6	b5	b4	b3	b2	b1	b0
DFEI8	10	b7	b6	b5	b4	b3	b2	b1	b0
FFEQ3	11	b7	b6	b5	b4	b3	b2	b1	b0
....	...	b7	b6	b5	b4	b3	b2	b1	b0
FFEQ0	14	b7	b6	b5	b4	b3	b2	b1	b0
DFEQ1	15	b7	b6	b5	b4	b3	b2	b1	b0
....	...	b7	b6	b5	b4	b3	b2	b1	b0
DFEQ8	1C	b7	b6	b5	b4	b3	b2	b1	b0
FFEI5	1D	b7	b6	b5	b4	b3	b2	b1	b0
FFEQ5	1E	b7	b6	b5	b4	b3	b2	b1	b0

FUNCTION	ADD	D7	D6	D5	D4	D3	D2	D1	D0
FFEI4	1F	b7	b6	b5	b4	b3	b2	b1	b0
FFEQ4	20	b7	b6	b5	b4	b3	b2	b1	b0
IF_frequency_shift	21	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
IF_frequency_shift	22	–	–	–	–	FS11	FS10	FS9	FS8

7.1.12 I²C-BUS WRITE PARAMETERS

Table 10 I²C-bus write parameters; 1-bit values

PARAMETER	BIT	VALUE	DESCRIPTION
Input format	INP	0	2's complement
		1	straight binary
Inversion demodulator	INVD	0	Q-branch = 0 – 1, 0, +1
		1	Q-branch = 0 + 1, 0, –1
Demodulator	DEM	0	by-pass mode
		1	normal mode
Half Nyquist filter	NYQ	0	filter in by-pass mode
		1	half Nyquist filter on
Roll-off factor	RLF	0	15% roll-off
		1	20% roll-off
Digital phase rotator	DPHR	0	off: pass through mode
		1	on
General reset	RST	0	normal operation
		1	reset (with automatic return to normal operation)
Offset	OFFS	0	off
		1	on
Outer loop activation (carrier recovery)	OUTE	0	outer loop inactive
		1	outer loop active
Analog switches	ANAS	0	open
		1	closed
1st and 2nd-order loop (inner loop)	FSOL	0	1st-order loop
		1	2nd-order loop
DAC current inversion	CARI	0	no inversion
		1	inversion
	CLKI	0	no inversion
		1	inversion
	AGCI	0	no inversion
		1	inversion

PARAMETER	BIT	VALUE	DESCRIPTION
Equalizer	PRESET	0	normal operation
		1	coefficient to zero (main tap to 1)
	EDFE	0	normal operation
		1	freeze coefficients of DFE part
	EFFE	0	normal operation
		1	freeze coefficients of FFE part
	EFC [fine AGC (equalizer freeze centre tap)]	0	normal operation
		1	freeze centre tap, no fine AGC
	EAR	0	automatic reset switched OFF
		1	automatic reset switched ON
	FFEL	0	5 taps in FFE part
		1	3 taps in FFE part

Table 11 I^2C write parameters; 2-bit values

PARAMETER	BITS		DESCRIPTION
Window size (lock detector)	WS1	WS0	
	0	0	256 symbols
	0	1	512 symbols
	1	0	1024 symbols
	1	1	2048 symbols
Output format	OUTB	OUTA	
	0	0	scheme 1
	0	1	scheme 2
	1	0	scheme 3
	1	1	scheme 4
DAC carrier recovery (maximum current)	CARB	CARA	
	0	0	50 µA
	0	1	100 µA
	1	0	150 µA
	1	1	200 µA
DAC clock recovery (maximum current)	CLKB	CLKA	
	0	0	50 µA
	0	1	100 µA
	1	0	150 µA
	1	1	200 µA
DAC AGC (maximum current)	AGCB	AGCA	
	0	0	50 µA
	0	1	100 µA
	1	0	150 µA
	1	1	200 µA

Table 12 I²C-bus write parameters; 3-bit values

PARAMETER	BITS			DESCRIPTION
	CONC	CONB	CONA	
Constellation	0	0	0	4-QAM
	0	0	1	16-QAM
	0	1	0	32-QAM
	0	1	1	64-QAM
	1	0	0	256-QAM

Table 13 Convergence step for the equalizer (DFE and FFE parts)

DSTP2 FSTP2	DSTP1 FSTP1	DSTP0 FSTP0	CONVERGENCE STEP (LOCK = 0)	CONVERGENCE STEP (LOCK = 1)
0	0	0	2^{-13}	2^{-15}
0	0	1	2^{-13}	2^{-14}
0	1	0	2^{-13}	2^{-13}
0	1	1	2^{-12}	2^{-15}
1	0	0	2^{-12}	2^{-14}
1	0	1	2^{-12}	2^{-13}
1	1	0	2^{-12}	2^{-12}
1	1	1	2^{-11}	2^{-15}

Table 14 I²C-bus write parameters; 4-bit values

PARAMETER	BITS				DESCRIPTION
	OUTF	TSEL2	TSEL1	TSEL0	
Output format	0	0	0	0	8 bits in parallel
	0	1	1	1	I/Q 8 bits multiplexed (equalizer output)
	1	x	x	x	semi-serial
Special test modes	0	x	0	1	DO7 to DO4 = carrier recovery DAC input; DO3 to DO0 = AGC DAC input
	0	x	1	0	DO7 to DO6 = fine AGC; DO5 to DO0 = clock recovery DAC input
	0	0	1	1	DO7 to DO0 = I and Q equal input (I/Q 8 bits multiplexed format)
	0	1	1	1	DO7 to DO0 = I and Q equal output (I/Q 8 bits multiplexed format)

7.1.13 I²C-BUS READ PARAMETERS

Table 15 I²C-bus read parameter; 1-bit values

PARAMETER	BIT	VALUE	DESCRIPTION
Lock detect	LK	0	no lock
		1	lock
Alarm equalizer	ALEQ	0	normal operation (alarm off)
		1	divergence detected (alarm on)

Table 16 I²C-bus read parameter; ADC carrier recovery; 4-bit value

PARAMETER	BITS				DESCRIPTION
ADC carrier recovery	CR03	CR02	CR01	CR00	
	b3	b2	b1	b0	carrier recovery: $V_{CARREC} = 0.25 + {}^{1}/_{16}V_{DDD}$ (8b3 + 4b2 + 2b1 + b0) V

Table 17 I²C-bus read parameter; ADC clock recovery; 4-bit value

PARAMETER	BITS				DESCRIPTION
ADC clock recovery	CL03	CL02	CL01	CL00	
	b3	b2	b1	b0	clock recovery: $V_{CLKREC} = 0.25 + {}^{1}/_{16}V_{DDD}$ (8b3 + 4b2 + 2b1 + b0) V

Table 18 I²C-bus read parameter; ADC AGC; 4-bit value

PARAMETER	BITS				DESCRIPTION
ADC AGC	AG03	AG02	AG01	AG00	
	b3	b2	b1	b0	AGC: $V_{AGC} = 0.25 + {}^{1}/_{16}V_{DDD}$ (8b3 + 4b2 + 2b1 + b0) V

Table 19 I²C-bus read parameter; 8-bit value

PARAMETER	BITS								DESCRIPTION
SER (1)	LE7	LE6	LE5	LE4	LE3	LE2	LE1	LE0	
	b7	b6	b5	b4	b3	b2	b1	b0	SER = f (b7 to b0)

Note

1. The bits LE7 to LE0 give the number of symbols falling inside the lock detector active areas. The count is made during an observation period (256 to 2048 symbols).
   To obtain more details about the SER estimation, refer to *"Application Note AN96048"*.

Table 20 I²C-bus read parameter; 12-bit value

PARAMETER	BITS	DESCRIPTION
IF_FREQ_SHIFT(1)	FS11 to FS0	frequency shift = f (FS11 to FS0)

Note

1. The bits FS11 to FS0 indicate the remaining frequency shift of the QAM spectrum (IF spectrum). This data is useful if the TDA8046H does not use the outer loop of carrier recovery (bit 'OUTE' of the I²C-bus table set to 0).
   To obtain more details about the frequency shift calculation, refer to the *"Application Note AN96048"*.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.3	6.0	V
V_{max}	maximum voltage on all pins		0	V_{DDD}	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	–	1.4	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	70	°C

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	50	K/W

10 DEMODULATOR AND HALF NYQUIST FILTER CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α	roll-off		–	15 or 20	–	%
	pass-band ripple		–	0.05	–	dB
	stop-band ripple		see Figs 5 and 6			
ISI_{power}	power inter-symbol interference (15% roll-off filter)	note 1	–	–43	–	dB
	power inter-symbol interference (20% roll-off filter)	note 1	–	–44	–	dB

Note

1. Definition of the power inter-symbol interference:

$$ISI_{power}(dB) = 10 \log \left[\frac{2 \times \sum_{k=1}^{(N_{conv}-1)/2} |C_{conv}(4k)|^2}{|C_{conv}(0)|^2} \right]$$

Where N_{conv} is the number of coefficients C_{conv}. $C_{conv}(k)$ represent the coefficient resulting from the convolution of the transmission and reception filters (K indicates the K^{th} coefficient).

The power ISI specified in Table 1 has been calculated on a filter resulting from the convolution of the TDA8046 filters and a truncated half-Nyquist filter with 57 T/4 taps for the 15% roll-off filter and 41 T/4 taps for the 20% roll-of filter (see "*Application note AN96048"* - Appendix B).

11 LOCK DETECTOR CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SNR_{lock}	signal-to-noise ratio to lock the demodulator	4-QAM	8	–	–	dB
		16-QAM	15	–	–	dB
		32-QAM	18	–	–	dB
		64-QAM	21	–	–	dB
		256-QAM	27	–	–	dB

12 CARRIER RECOVERY CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Carrier recovery detector						
CARRIER RECOVERY: BIAS CURRENT FOR DACS SET TO 37.5 µA						
K_d	detector constant	SNR = 21 dB for 64-QAM constellation	–	$3I_{CAR}$	–	µA/rad
		SNR = 27 dB for 256-QAM constellation	–	$6.05I_{CAR}$	–	µA/rad
Δf_{CAR}	frequency range		$\pm 0.017 r_s$	–	–	MHz
$f_{n(inner)}$	loop bandwidth of inner loop	r_s = 5 Msym/s	10	–	–	kHz
$f_{n(outer)}$	loop bandwidth of outer loop		–	–	$0.3f_{n(inner)}$	kHz
I_{zero}	zero current of DAC		–100	–	+100	nA
I_{CAR}	maximum DAC output current (programmable)		50	–	200	µA
f_{DAC}	DAC sampling rate		–	r_s	–	MHz
CARRIER RECOVERY DAC OUTPUT CURRENTS DURING LOCK						
$I_{oCARlock}$	mean output current		–	$\frac{1}{2}I_{CAR}$	–	µA
$\Delta I_{oCARlock}$	matching of output currents		–2.5	–	+2.5	%
CARRIER RECOVERY DAC OUTPUT CURRENTS DURING UNLOCK						
$I_{oCARunlock}$	mean output current		–	I_{CAR}	–	µA
$\Delta I_{oCARunlock}$	matching of output currents		–2.5	–	+2.5	%

13 CLOCK RECOVERY CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock recovery detector						
CLOCK RECOVERY: BIAS CURRENT FOR DACS SET TO 37.5 µA						
K_d	detector constant	SNR = 21 dB for 64-QAM constellation; SNR = 27 dB for 256-QAM constellation	–	$0.24I_{CLK}$	–	µA/rad
Δf_{CLK}	frequency range		100	–	–	ppm
f_n	natural frequency		–	400	–	Hz
$I_{CLK(max)}$	maximum DAC output current (programmable)		50	–	200	µA
f_{DAC}	DAC sample rate		–	r_s	–	MHz
CLOCK RECOVERY DAC output currents						
$I_{oCLKlock}$	mean output current		–	I_{CLK}	–	µA
$\Delta I_{oCLKlock}$	matching of output currents		–2.5	–	+2.5	%

14 AGC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC detector						
AGC DETECTOR: BIAS CURRENT FOR DACS SET TO 37.5 µA						
ΔR_{AGC}	AGC range of detector		±20	–	–	dB
I_{zero}	zero current		–100	–	+100	nA
$I_{AGC(max)}$	maximum DAC output current (programmable)		50	–	200	µA
f_{DAC}	DAC sample rate		–	r_s	–	MHz
AGC DAC output currents						
I_{oAGC}	mean output current	in lock	–	$\frac{1}{14}I_{AGC}$	–	µA
		unlock	–	I_{AGC}	–	µA
ΔI_{oAGC}	matching of output current		–5		+5	%

15 INTEGRATED LOOP AMPLIFIERS CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Integrated loop amplifiers						
LOOP AMPLIFIERS						
G_{OL}	open loop gain		–	60	–	dB
G_B	gain bandwidth product		–	1	–	MHz
V_{ref}	reference voltage		–	2.5	–	V
V_o	output voltage		$0.1V_{DDA}$	–	$0.9V_{DDA}$	V
$R_{L(VSSD)}$	load to ground		5	–	–	kΩ
$R_{L(VDDD)}$	load to supply		6.5	–	–	kΩ
ANALOG SWITCHES						
Z_{SW}	switch impedance	closed	–	5	–	kΩ
		open	10	–	–	MΩ

16 CHARACTERISTICS OF DIGITAL INPUTS AND OUTPUTS

$V_{DDD} = V_{DDA} = 5$ V; $V_{DDD(core)} = 3.3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock outputs: CLKADC and CLKSDV						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DDD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DDD}$	–	V_{DDD}	V
T_{CLK}	cycle time		35	–	–	ns
t_w	pulse width	40 : 60 duty cycle	14	–	–	ns
t_r	rise time	$C_L = 30$ pF	–	–	6	ns
t_f	fall time	$C_L = 30$ pF	–	–	6	ns
R_L	load resistance		1	–	–	kΩ
Clock input: CLK						
$V_{i(rms)}$	input voltage level (RMS value)	sine wave	100	–	–	mV
T_{CLK}	cycle time		35	–	–	ns
t_w	pulse width	40 : 60 duty cycle	14	–	–	ns
R_{source}	source resistance		–	–	50	Ω
Digital inputs: DIN8 to DIN0						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	High level input voltage		2.0	–	–	V
t_{SU}	set-up time		15	–	–	ns
t_{HD}	hold time		0	–	–	ns
C_L	load capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs: DO1 to DO0 with respect to CLKOUT for semi-serial mode						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DDD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DDD}$	–	V_{DDD}	V
t_{od}	output delay time		–	–	7	ns
t_{oHD}	output hold time		–	–	10	ns
C_L	load capacitance	additional	2	–	30	pF
Digital outputs: DO7 to DO0 with respect to CLKSDV for 8-bit parallel mode						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DDD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DDD}$	–	V_{DDD}	V
t_{od}	output delay time		–	–	22	ns
t_{oHD}	output hold time		–	–	22	ns
C_L	load capacitance	additional	2	–	30	pF
Digital outputs: DO7 to DO0 with respect to CLKOUT for I/Q multiplexed mode						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DDD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DDD}$	–	V_{DDD}	V
t_{od}	output delay time		–	–	22	ns
t_{oHD}	output hold time		–	–	22	ns
Loop amplifier						
V_o	output voltage level		$0.1V_{DDA}$	–	$0.9V_{DDA}$	
G_v	DC voltage gain (open loop)		–	60	–	dB
G_B	gain bandwidth product		1	–	–	MHz
R_L	load resistance		5	–	–	KΩ

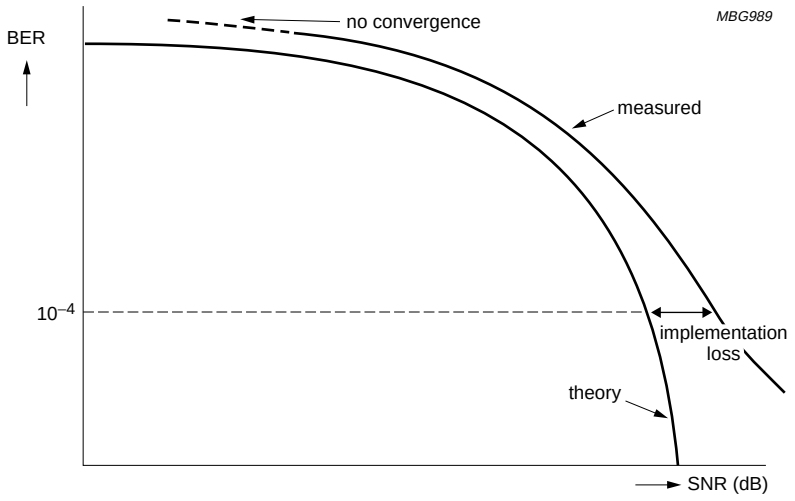


Fig.31 Definition of the Implementation Loss.

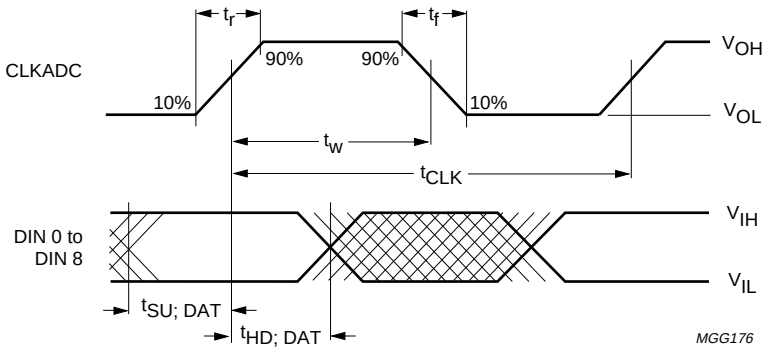


Fig.32 CMOS input data timing diagram.

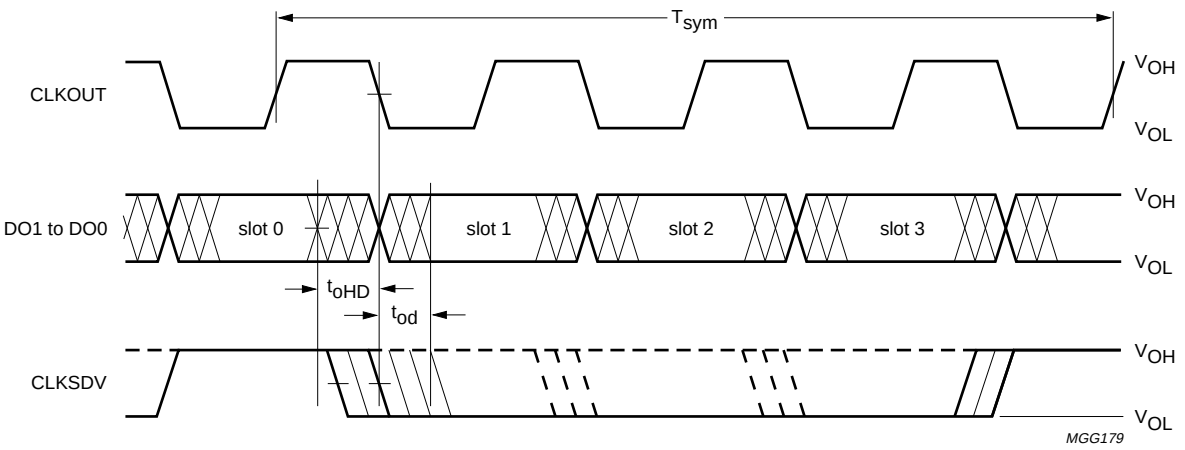


Fig.33 CMOS semi-serial mode timing diagram.

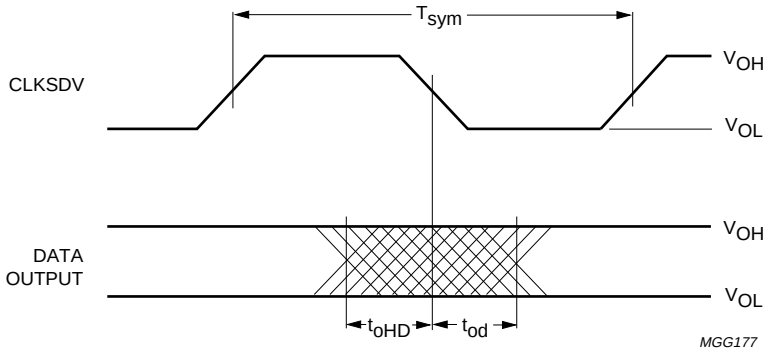


Fig.34 CMOS 8-bit symbol in parallel mode timing diagram

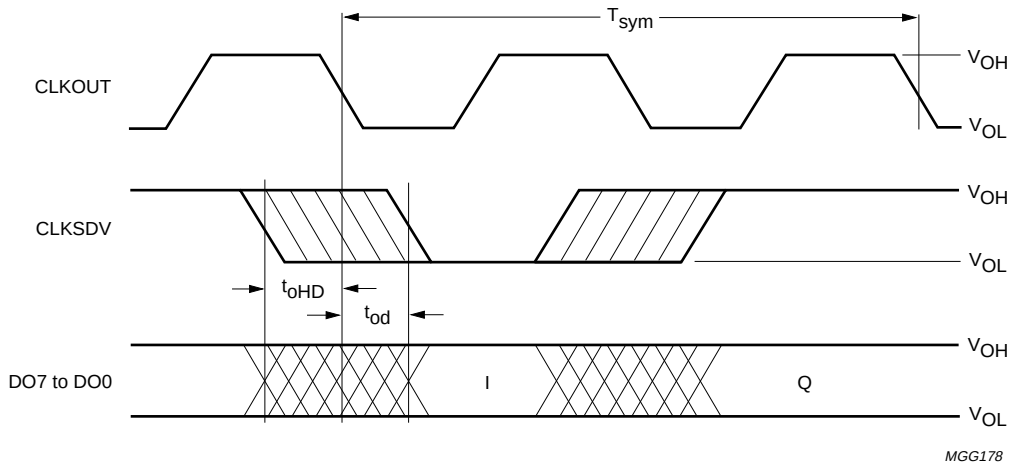
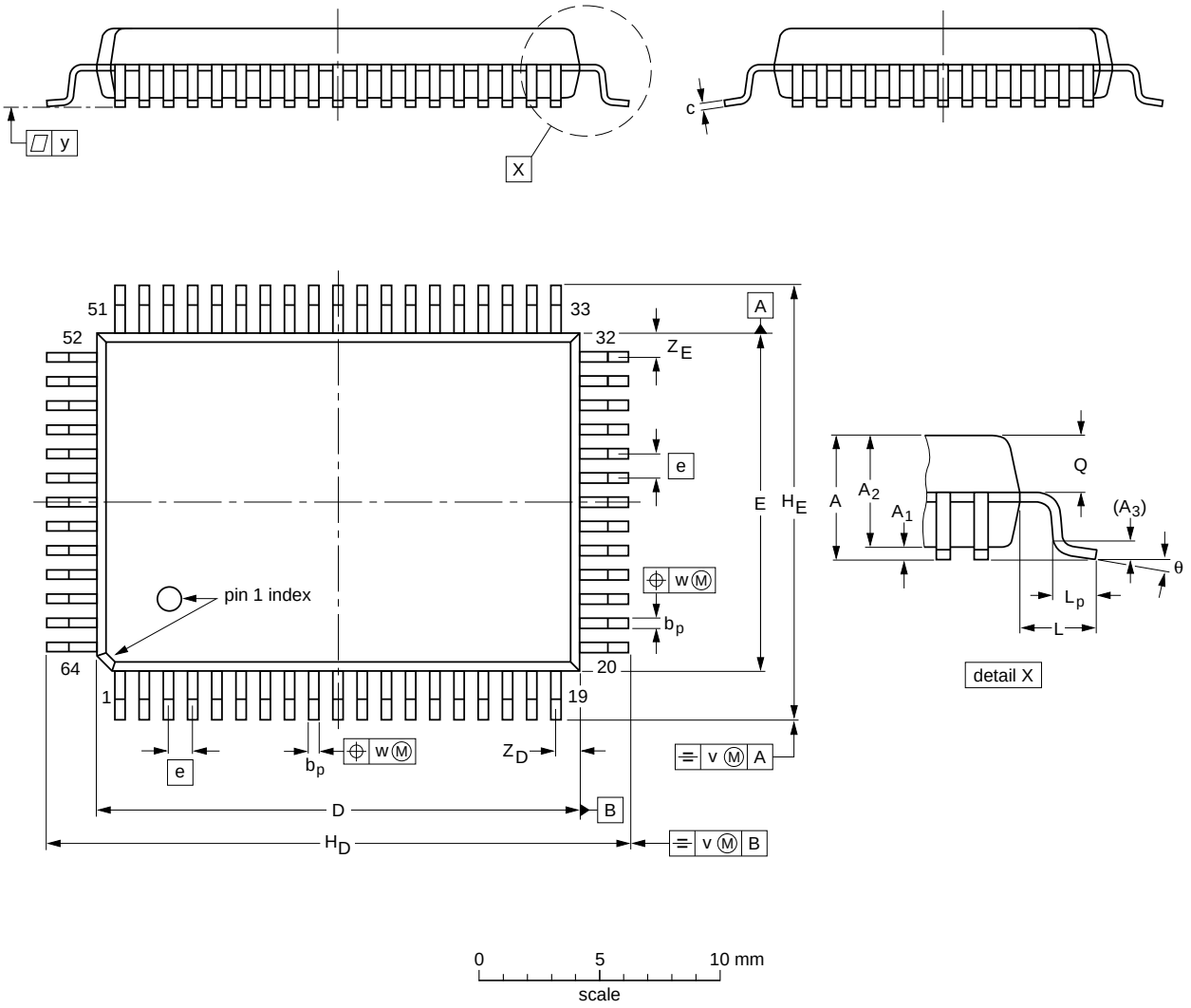


Fig.35 CMOS I and Q multiplexed timing diagram.

17 PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

18.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

18.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

20 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

21 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 247 9145, Fax. +7 095 247 9144

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 537021/1200/02/pp48 Date of release: 1996 Nov 19 Document order number: 9397 750 01499

Let's make things better.

Philips Semiconductors

PHILIPS